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# Accumulator Based 3-Weight Pattern Generation for Complex Large Scale Integration Packages

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## ABSTRACT

We describe a method for on-chip generation of weighted test sequences for synchronous sequential circuits. For combinational circuits, three weights, 0, 0.5 and 1, are sufficient to achieve complete coverage of stuck-at faults, since these weights are sufficient to reproduce any specific test pattern. For sequential circuits, the weights we use are defined based on subsequences of a deterministic test sequence. Such weights allow us to reproduce parts of the test sequence, and help ensure that complete fault coverage would be obtained by the weighted test sequences generated. In this paper an accumulator-based 3-weight test pattern generation scheme is presented. The proposed scheme copes with the inherent drawbacks of the scheme proposed more precisely. First, it does not impose any requirements about the design of the adder i.e., it can be implemented using any adder design and then it does not require any modification of the adder; and hence it does not affect the operating speed of the adder. Furthermore, the proposed scheme compares favorably to the scheme proposed in terms of the required hardware overhead. The weighted random test pattern generation represents a significant departure from classical methods of generating test sequences for complex large scale integration packages. The virtue of this technique is its simplicity and the fact that test-generation time is virtually independent of or gates in the logic package to be tested. This technique can be used both in a conventional tester and in a tester where the weighted random test pattern generation is implemented in hardware.

**Keywords: Sequential Circuits , Combinational Circuits , Patterngeneration**

## I.INTRODUCTION

Arithmetic operations include operations of adding, subtracting, multiplying, dividing, comparing, and finding a square root. The multiplication operation is the second operation in the computers after the addition. There are several methods of multiplication acceleration: a way to change the encoding system of multipliers, which can reduce the amount of summating partial products (Booth's algorithm), using more efficient variants of partial products adding that exclude time- consuming spreading of transfer and the method of parallel computing of all partial products. All these three approaches are usually implemented using combinational devices. Parallel computation of partial products takes place in all multiplication schemes. The difference is mainly observed in the method of summing up the obtained partial products, and from this position, the usage of multiplication schemes can be divided into matrix-like and multilayer with a tree structure. The difference between matrix and multilayered multipliers is expressed in the number of one-bit adders used, their type, and the method of spreading the transfers that arise in the process of summation. The most well-known matrix multipliers are: Brown's multiplier, a multiplier with horizontal spreading of transfer and multipliers that are constructed using Baugh-Wooley's [13] and Pezaris's [14] algorithms for multiplying binary numbers in complementary codes. In matrix multipliers, the

summation is made by a matrix of adder, which consists of successive rows of one-bit adders with transfer saving. As the data moves down the array of adders, each line of the adder with transfer saving adds another partial product to the sum of partial products. With high performance, the important achievements of matrix multipliers are their regularity, which is especially significant when implementing such multipliers in the form of an integrated circuit. On the other hand, such circuits occupy a large area on the crystal of the chip, and with the increase of the bit-capacity of multipliers, this area increases in proportion to the square of the number of bit-capacity.

## II. LITERATURE REVIEW

**Irith Pomeranz and Sudhakar M. Reddy-"Built-In Generation of Weighted Test Sequences for Synchronous Sequential Circuits"**

**Description:** Here the description of this method is used for on-chip generation of weighted test sequences for synchronous sequential circuits. The weights we used were defined based on subsequences of a deterministic test sequence. The use of a deterministic test sequence to define the weights allowed us to reproduce parts of the test sequence, and helped ensure that complete fault coverage would be obtained. It described a procedure for defining a set of weights from which weight assignments can be constructed, a procedure for selecting weight assignments so as to detect target faults, and presented experimental results to demonstrate that complete fault coverage can be achieved by this method. It also investigated the tradeoff between the number of weight assignments and the number of observation points required to achieve complete fault Coverage. The use of pure-random sequences as part of the weight scheme, followed by the synthesis of the on-chip test generation hardware, is the subject of future work.

**Disadvantages of existing system:** This method is not applicable when a single test sequence is given for the circuit.

**Advantages of our proposed system**: In accumulator based 3-weight pattern generation is easy to used and applicable for a single test sequence is given circuit.

**Ioannis Voyiatzis- "An Accumulator-Based Compaction Scheme for Online BIST of RAMs"**

**Description :** The utilization of accumulator modules for output data compaction in symmetric transparent BIST for RAMs is proposed. It is widely accepted by the test community that the utilization of modules that typically exist in the circuit, e.g., accumulators or arithmetic logic units, for BIST test pattern generation and/or response verification possesses advantages, It is shown that in this way the hardware overhead, the complexity of the controller, and the aliasing probability are considerably reduced.

**Disadvantages of existing system:** Lower hardware overhead and elimination of the need for multiplexers in the circuit path; furthermore, the modules are exercised. Therefore, faults existing in them can be discovered.

**Advantages of Our Proposed systems:** The comparison will be performed with respect to the hardware overhead and no elimination of the need for multiplexers in the circuit path.

**Katarzyna Radecka, Janusz Rajski-"Arithmetic Built-In Self-Test for DSP Cores"**

**Description** It is demonstrated how components are themselves tested, and subsequently used to perform more complex testing functions. The need for extra hardware is either entirely eliminated or drastically

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reduced, test vectors can be easily distributed to different modules of the system, test responses can be collected in parallel, and there is virtually no performance degradation.

**Disadvantages of existing system:** The existing data-path BIST schemes are unfortunate examples of having sophisticated modules on the chip, but remain unable to translate this advantage into efficient nonintrusive testing schemes.

**Advantages our proposed systems:** Redesign of the accumulator is imposed, thus resulting in reduction in test application time.

## III. PROPOSED SYSTEM

Generally, the accumulator-based compaction technique uses an accumulator to generate a composite fault signature for a circuit under test. The error coverage for this method has been previously analyzed. We describe an alternative technique for calculating the error coverage of accumulator-based compaction using the asymmetric error model. This technique relies on the central limit theorem of statistics and can be applied to other count-based compaction schemes. The data paths of most contemporary general and special purpose processors include registers, adders and other arithmetic circuits. If these circuits are also used for built-in self-test, the extra area required for embedding testing structures can be cut down efficiently. Several schemes based on accumulators, subtracters, multipliers and shift, resisters have been proposed and analyzed in the past for parallel test response compaction, whereas some efforts have also been devoted in the bit-serial response compaction case.

The utilization of accumulators for time compaction of the responses in built-in self test environments has been studied by various researchers. One of the well-known problems of time compactors is aliasing, i.e. the event that a series of responses containing errors result in a signature equal to that of an error-free response sequence. In this paper we propose a scheme to reduce aliasing in accumulator based compaction environments. With the proposed scheme, the aliasing probability tends to zero, as the number of the patterns of the test set increases.

We use a pseudo random generator made using Linear Feedback Shift Register (LFSR). These patterns generated using LFSR have all the desirable properties of random numbers, but are algorithmically generated by the hardware pattern generator and are therefore repeatable, Which is essential for BIST? We no longer cover all the 2^ncombinations, but a large number of test pattern sequences will still be necessary to attain sufficient fault coverage.In general, pseudo random pattern generation requires more patterns than completely deterministic Automatic Test Pattern Generation (ATPG), but obviously, fewer than the exhaustive testing. However, it was found that the stuck-fault coverage rises in a logarithmic fashion towards hundred percentage, but at the cost of enormous numbers of random patterns. On top of it, certain circuits are random pattern resistant circuits in that they do not approach full fault coverage with an unbiased random pattern. Such circuits require extensive insertion of testability hardware or a modification of random pattern generation to ‗weighted pseudo random pattern generation' in order to obtain an acceptable fault percentage.

### ACCUMULATOR CELL

The main object of the weighted pattern generation is an accumulator cell. To implement the accumulator in the proposed weighted pattern generation scheme is based on presented in Figure.

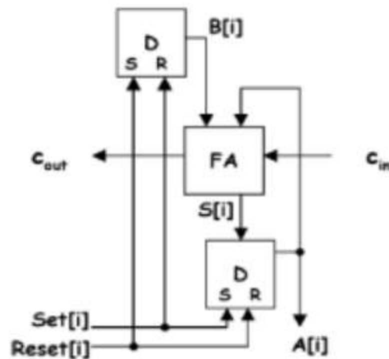


**Figure 1:Shows Accumulator Cell**

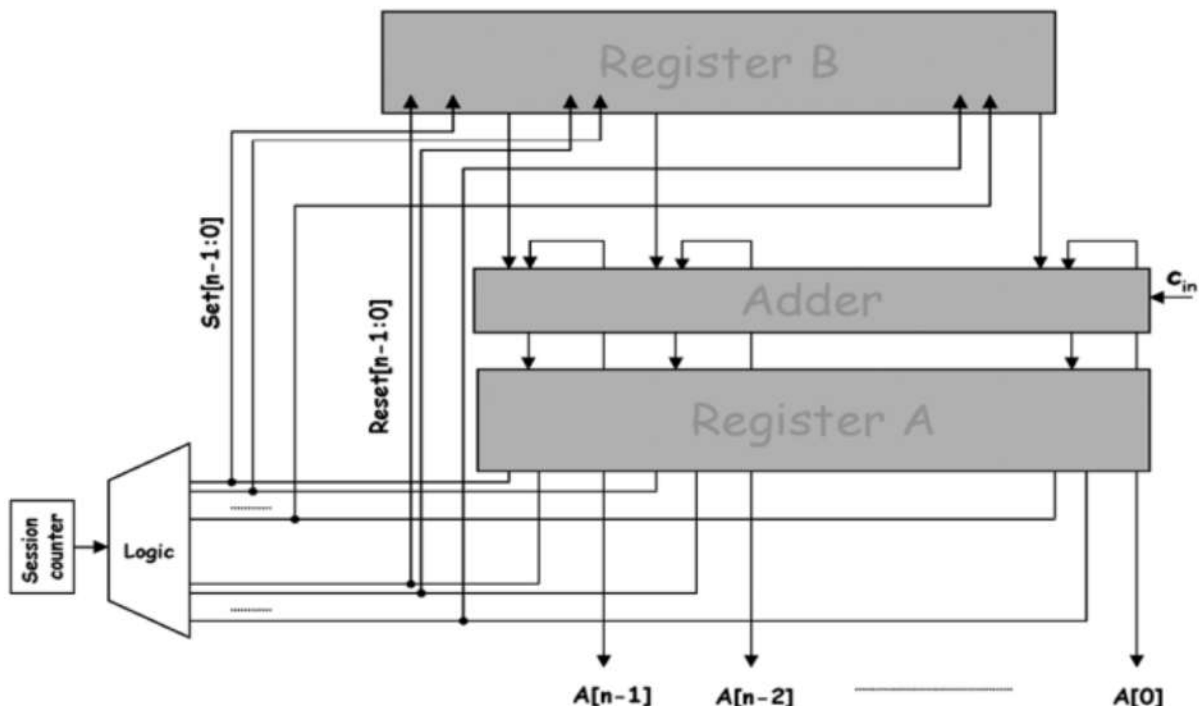


**Figure 2:Shows Proposed Schema**

All schemes require the application of the session counter, required to alter among the different weight sessions. The number of test patterns applied and the proposed scheme is the same, since the test application algorithms that have been invented and applied, Methods to generate weighted pseudo-random patterns for combinational circuits that can be extended to sequential circuits this method is based on the use of three weights, 0, 0.5 and 1. A weight assignment associates one of these weights with every primary input of the circuit. A preselected number of patterns Nis applied under every weight assignment. A weight of 0.5 assigned to an input iby a weight assignment w implies that pseudo-random patterns are applied to input iwhile Ntest patterns are applied to the circuit; a weight of 0 assigned to input i implies that input iis held at 0 constantly for the N test patterns and a weight of 1 assigned to input i implies that input i is held at 1 constantly for the N test patterns. The weight assignments are based on a deterministic test

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set. Each weight assignment is obtained by intersecting a subset of deterministic test patterns. The intersection of identical values, 0 or 1, yields a weight of 0 or 1, respectively.

## IV. RESULTS AND DISCUSSION

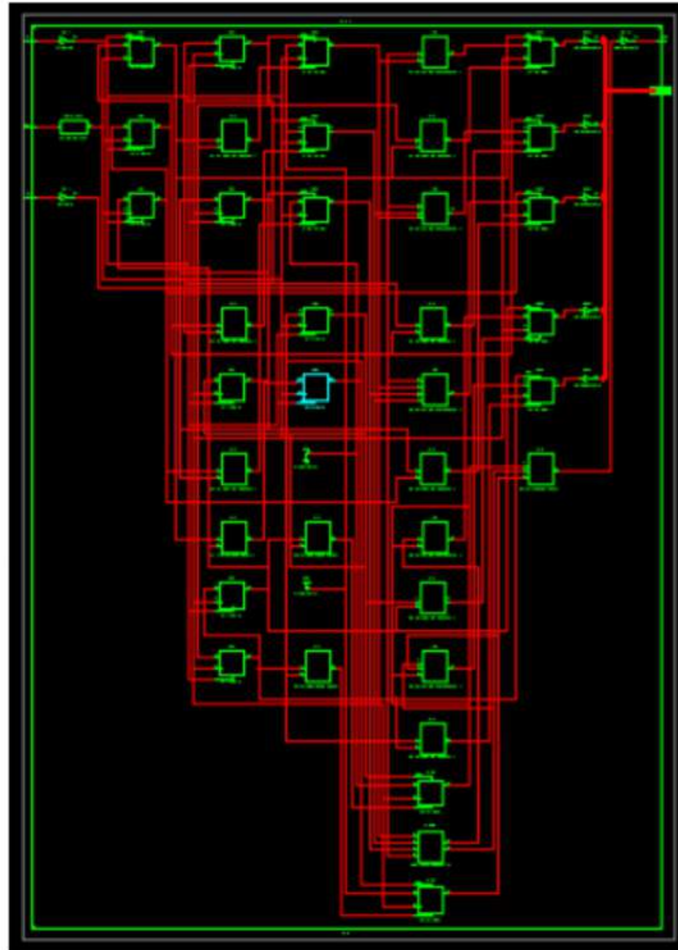

**Figure 3 : Proposed Shema Technological View**

1.WCA pattern generators designed by MWCARGO achieved 100 percent coverage of testable stuck-at faults for benchmark circuits with random-pattern-resistant faults.

2. This method is significantly different from weighted pattern generation and can guarantee testing of all hard-to-detect faults without expensive test point insertion. Experimental results on common benchmark net-lists demonstrate that the fault coverage of the proposed pattern generator is significantly higher compared to conventional pattern generation techniques. The design technique for the logic mapper is unique and can be used effectively to improve existing pattern generators for combinational logic and scan-based BIST structures.

The data for some of the ISCAS'85 and ISCAS'89 benchmarks are presented, where the same fault coverage, i.e., 100% is targeted. We present the number of test patterns and hardware Overhead for the

proposed scheme. it is trivial to see that the proposed scheme presents an important decrease in the hardware overhead, while the number of tests is comparable It is interesting to note that the hardware overhead with respect to the hardware overhead of the benchmarks is practical. which sometimes exceeds the benchmark hardware (c2670, s5378, s9234, s13207, s15850,s38584). The average increase in the number of tests, while the average decrease in hardware overhead to 98%.

Finally, we have presented an accumulator-based 3-weight (0, 0.5, and 1) test-per-clock generation scheme, which can be utilized to efficiently generate weighted patterns without altering the structure of the adder. Comparisons with a previously proposed accumulator-based 3-weight pattern generation technique and it indicates that the hardware overhead of the proposed scheme is lower, while at the same time no redesign of the accumulator is imposed, thus resulting in reduction in test application time. Comparisons with scan based schemes show that the proposed schemes results in lower hardware overhead. Finally, comparisons with the accumulator- based scheme proposed and reveal that the proposed scheme results in significant decrease in hardware overhead.

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