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High Speed Approximate 2n bit multiplier with n bit multipliers to reduce the design complexities

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ABSTRACT

The structures of matrix and tree-like multipliers of binary numbers were reviewed and their system characteristics were show more affects on the digital signal processing applications. Approximate computing exploits the fact that many applications are inherently error resilient. In order to reduce power consumption approximate circuits such as multipliers have been employed in these applications. However, most current approximate multipliers are based on ad hoc circuit structures and, for automated circuit approximation methods, large efficient designs are difficult to find due to the increased search space. Here in this project we design a larger multiplier by using smaller multipliers such the approximation is done at the stage of partial product Addition. The internal structure of incomplete one-bit adder adders has been proposed, which allowed reducing the area of multipliers and increases the speed of operation. A comparative analysis of the obtained results was made it possible for a designer to choose the optimal structure of the multiplier to accomplish the task of hardware multiplication of binary numbers with given system characteristics. The entire designs was synthesized and simulated in Xilinx ISE with verilog HDL coding.

Keywords: Multipliers , Matrix ,hoc Circuits

I.INTRODUCTION

Arithmetic operations include operations of adding, subtracting, multiplying, dividing, comparing, and finding a square root. The multiplication operation is the second operation in the computers after the addition. There are several methods of multiplication acceleration: a way to change the encoding system of multipliers, which can reduce the amount of summating partial products (Booth's algorithm), using more efficient variants of partial products adding that exclude time- consuming spreading of transfer and the method of parallel computing of all partial products. All these three approaches are usually implemented using combinational devices. Parallel computation of partial products takes place in all multiplication schemes. The difference is mainly observed in the method of summing up the obtained partial products, and from this position, the usage of multiplication schemes can be divided into matrix-like and multilayer with a tree structure. The difference between matrix and multilayered multipliers is expressed in the number of one-bit adders used, their type, and the method of spreading the transfers that arise in the process of summation. The most well-known matrix multipliers are: Brown's multiplier, a multiplier with horizontal spreading of transfer and multipliers that are constructed using Baugh-Wooley's [13] and Pezaris's [14] algorithms for multiplying binary numbers in complementary codes. In matrix multipliers, the summation is made by a matrix of adder, which consists of successive rows of one-bit adders with transfer saving. As the data moves down the array of adders, each line of the adder with transfer saving adds another partial product to the sum of partial products. With high performance, the important achievements

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of matrix multipliers are their regularity, which is especially significant when implementing such multipliers in the form of an integrated circuit. On the other hand, such circuits occupy a large area on the crystal of the chip, and with the increase of the bit-capacity of multipliers, this area increases in proportion to the square of the number of bit-capacity.

II. LITERATURE REVEIW

V. Gryga, Y. Nykolaichuk, N. Vozna, B. Krulikovskyi "Synthesis of a microelectronic structure of a specialized processor for sorting an array of binary numbers" MEMSTECH 2017. – Lviv-Svalyava, Ukraine, 2017. – P. 170-173.

Sorting is one of the common problems of data processing and is generally understood as a problem of placing elements of disordered set of values of data sets in order of monotonic increase or decrease [1]. Ensure the implementation of this operation in real time is possible on specialized means and which architecture fully reflects the structure of the sorting algorithm and focused on implementation as programmable integrated circuits (FPGA) or very large scale integrated circuits (VLSI). Using specialized equipment gives an ability to perform with high efficiency sorting operation of a given algorithm in relation to the universal computer system. There is a significant number of known algorithms for sequential and parallel sorting data sets that can be implemented in hardware **Domain Specific Accelerator Processors:** In the domain specific platforms, several research works have been carried on implementation of simpler cores for optimization rather than having application specific processors. There has been work on simple programmable processors used for application specific mapping.

B. Krulikovskyi, A. Davletova, V. Gryga, Y. Nykolaichuk "Synthesis of Components of High Performance Special Processors of Execution of Arithmetic and Logical Operations Data Processing in Theoretical and Numerical Basis Rademacher"

The analysis of classical component building for such processors shows that the most important task for optimizing their system characteristics is to achieve maximum performance. In this case, the important component is multi-bit adder implemented using binary system. It is a basic element in accumulators, ALU and modular arithmetic devices: squares, vector-matrix multipliers and modular exponentiation devices. The analysis of the classical implementation such components show that they are characterized by a number of functional limitations, because they were focused on building small-bit processors (32 bit). Known acceleration methods for summing and multiplication characterized by a significant increase in hardware complexity and irregularity building patterns for multi-bit processors with increasing number of bits (1024, 2048 bit).

This significantly limits the effective application of known component implementations of adders for FPGA The disadvantage of binary half-adder is a big hardware complexity due to the presence of five logic elements. The use of such half-adder in multi-combinational adders, for example, in a 1024-bit data encryption processors, leading to significant relevant hardware complexity. Another disadvantage of the half-adder is a low speed, due to the presence of three serially connected logic elements in a matching circuit, that generates output sum of one-digit half-adder, which leading to lower speed of under multi-adders when used as a base component. In the onedigit half-adder large hardware complexity and low speed, due to the presence of the logical element "excluding OR".

R. Dunets, V. Gryga Spatio-temporal synthesis of transformation matrix of reverse fast cosine transformation CADSM'2015. – Lviv - Poljana, Ukraine, 2015. - pp. 45-49.

There is an approach to design of algorithmic operational devices (AOD), specialized hardware with the use of flow graph of algorithm that provides the direct representation of executable algorithm to the

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structure of physical device, where the tops of the graph are replaced by combinational circuits and arcs - by the data channels. Also, the methodology of design of conveyer devices on the basis of "projection of functional operators" that allow designing the single-channel and multichannel specialized devices with the use of the specialized memory is known.

III. PROPOSED SYSTEM

High computation performance at low power consumption is one of persistent design requirements in many applications, such as image processing, recognition and machine learning. The exactly numerical outputs are not necessary due to the error tolerance nature of these applications. Approximate computing is a promising approach to reduce design costs by exploiting the accuracy relaxation in error-tolerant applications, while still producing sufficiently exact results. Approximate circuit mainly discusses basic arithmetic units, such as the approximate 8×8 multiplier usually used in error tolerant applications. Many works have explored approximate multipliers. A multiplier design is introduced using a tree compressor in to reduce rows of the partial product matrix by half. In, approximate multipliers are explored using inexact half-adder, full-adder and 4:2 compressor. A bit significance-driven logic compression for approximate multipliers is discussed to reduce partial products. The strategies of inexact compression have introduced in, while the input to a compressor is limited. An approximate multiplier design is explored using an error recovery approach implemented by a conventional adder that costs a large delay. A conventional multiplier generally involves three steps: partial product generation, partial product reduction and carry propagation addition. The power consumption is dominated by the second step. where XOR-rich circuits, compressors are used. To compress partial products using low-cost circuits, we propose an inexact compressor cells called inexact adders.

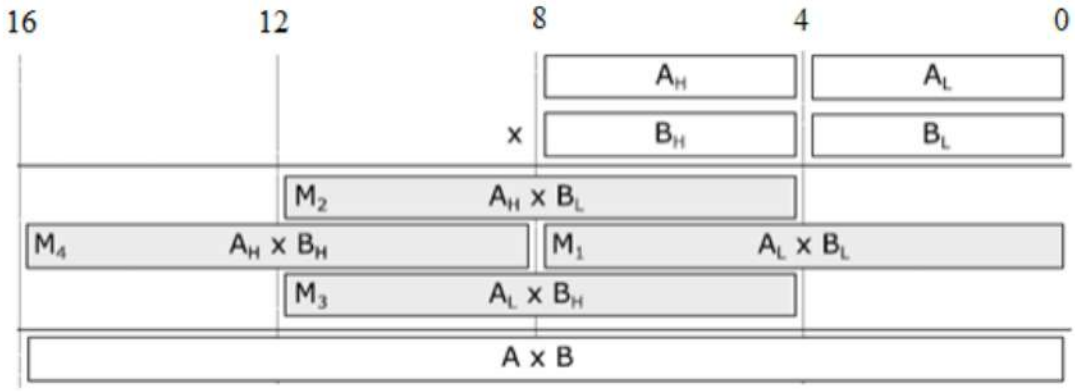

Figure 1:Shows Construction of a 2n × 2n multiplier from four n × n multipliers.

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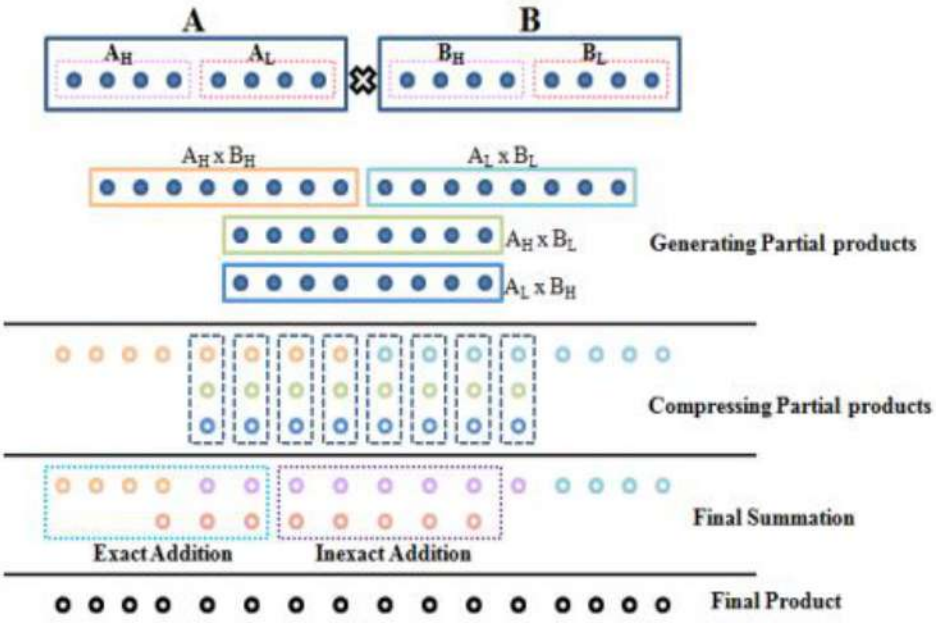

Figure 2 : Shows Proposed Multiplier Design

V. RESULTS AND DISCUSSION

Brauns_multiplier_8bit Project Status (01/12/2019 - 12:42:24)			
Project File:	multiplying_binary_numbers.xise	**Parser Errors:**	No Errors
Module Name:	Brauns_multiplier_8bit	**Implementation State:**	Synthesized
Target Device:	xc3s100e-5vq100	**• Errors:**	
Product Version:	ISE 14.7	**• Warnings:**	
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	72	960	7%
Number of 4 input LUTs	126	1920	6%
Number of bonded IOBs	32	66	48%

```
Delay:               21.132ns (Levels of Logic = 16)
  Source:            a<0> (PAD)
  Destination:       p<14> (PAD)

  Data Path: a<0> to p<14>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             15   1.106   1.016  a_0_IBUF (a_0_IBUF)
     LUT4:I0->O             2   0.612   0.532  g1/cout1 (c<0>)
     LUT4:I0->O             2   0.612   0.532  g8/cout1 (c<7>)
     LUT4:I0->O             2   0.612   0.532  g15/cout1 (c<14>)
     LUT4:I0->O             2   0.612   0.532  g55/cout1 (c<21>)
     LUT4:I0->O             2   0.612   0.532  g28/cout1 (c<28>)
     LUT4:I0->O             2   0.612   0.532  g35/cout1 (c<35>)
     LUT4:I0->O             2   0.612   0.532  g42/cout1 (c<42>)
     LUT4:I0->O             2   0.612   0.532  g49/cout1 (c<49>)
     LUT3:I0->O             2   0.612   0.532  g50/cout1 (c<50>)
     LUT3:I0->O             2   0.612   0.532  g51/cout1 (c<51>)
     LUT3:I0->O             2   0.612   0.532  g52/cout1 (c<52>)
     LUT3:I0->O             2   0.612   0.532  g53/cout1 (c<53>)
     LUT3:I0->O             2   0.612   0.532  g54/cout1 (c<54>)
     LUT4:I0->O             1   0.612   0.357  g56/Mxor_sum_xo<0>1 (p_14_OBUF)
```

Figure 3 : Shows the Brauns Multiplier and Delays

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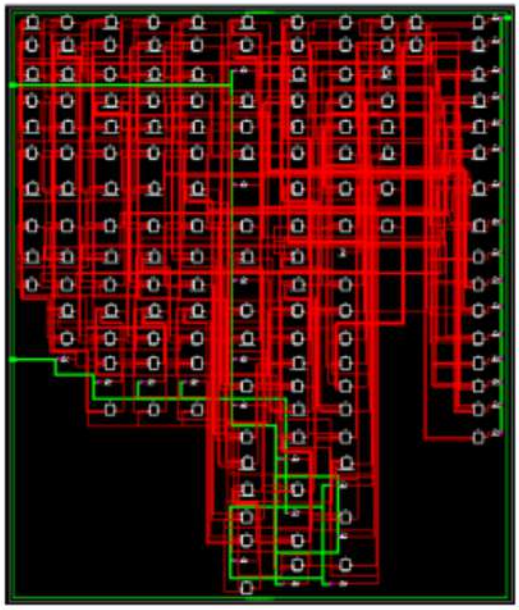

Figure 4: Shows the Technical Schematic

As a result of researching of the structures of matrix and tree-like algorithms of binary multiplication, their hardware, time and electrical characteristics were analyzed. With the use of pyramidal adders on the base of incomplete one-bit adders, it was possible to reduce the number of logical elements in adders. The internal structure of incomplete one-bit adder and pyramidal adder has been proposed, which allowed reducing the area of multipliers and increases the speed of operation. We demonstrated how to relatively quickly construct a high-quality set of non dominated 2n-bit approximate multipliers provided that we have a reasonable database of n-bit approximate multipliers. To enhance the performance in terms of delay we use approximation scheme. By this we can reduce the delay. The results of the synthesis of developed Verilog HDL models and is implemented in XILINX ISE.

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