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High Speed low power Precharge CAM design using hybrid self controlled

G.S.Neeraj prasad naidu[1],S. Imam Valli[2]
PG Scholar[1], Asst. Professor[2]
Department of Electronics and Communication Engineering
Golden Valley Integrated Campus
Angallu, Madanapalli, Andhra Pradesh, India

ABSTRACT

Content-addressable memory (CAM) is a prominent hardware for high-speed lookup search, but consumes larger power. Traditional NOR and NAND match-line (ML) architectures suffer from a short circuit current path sharing and charge sharing respectively during precharge. The recently proposed precharge-free CAM suffers from high search delay and the subsequently proposed self-controlled precharge-free CAM suffers from high power consumption. This paper presents a hybrid self-controlled precharge-free (HSCPF) CAM architecture, which uses a novel charge control circuitry to reduce search delay as well as power consumption. The proposed and existing CAM ML architectures were developed using CMOS 45nm technology node with a supply voltage of 1 V. Simulation results show that the proposed HSCPF CAM-type ML design reduces power consumption and search delay effectively when compared to recent precharge-free CAM-type ML architectural designs.
Keywords: Content-addressable memory, low power, match-line, precharge-free, search delay

I.INTRODUCTION

Content-addressable memory (CAM) compares stored lookup table data against search data parallel within a single clock cycle [1, 2] and returns the address of the matched data through match-line sense amplifier (MLSA). This parallel search scheme of CAM surmounts the software-based search algorithms for all the highspeed applications such as radix tree [3], image processing [4], 5G communication network [5], mobile devices [6], IP routing [7], gray coding [8] and so on. Parallel hardware activity of CAM exhibits high performance, but consumes large power. Hence, designing the CAM for a reduced power consumption and better performance becomes a challenging task. CAM cells arranged in a single row form one CAM word [9]. Each CAM word is connected to a single match-line (ML) as shown in Figure 1. Prior to the search operation, all the MLs are precharged to high voltage [10]. During search operation, only a single word is matched with search word and the corresponding ML needs to hold the charge. All the other mismatched MLs will be discharged. This regular precharging and discharging of MLs consume considerable dynamic power in CAM. Here, we briefly review a few techniques for power reduction of CAM. Many works were reported to reduce the switching power consumption involved in precharging the MLs. Some researchers worked on segmenting the word into subwords. The segments are arranged in parallel and hierarchical architectures in [11], respectively. The word is divided into master and slave paths.

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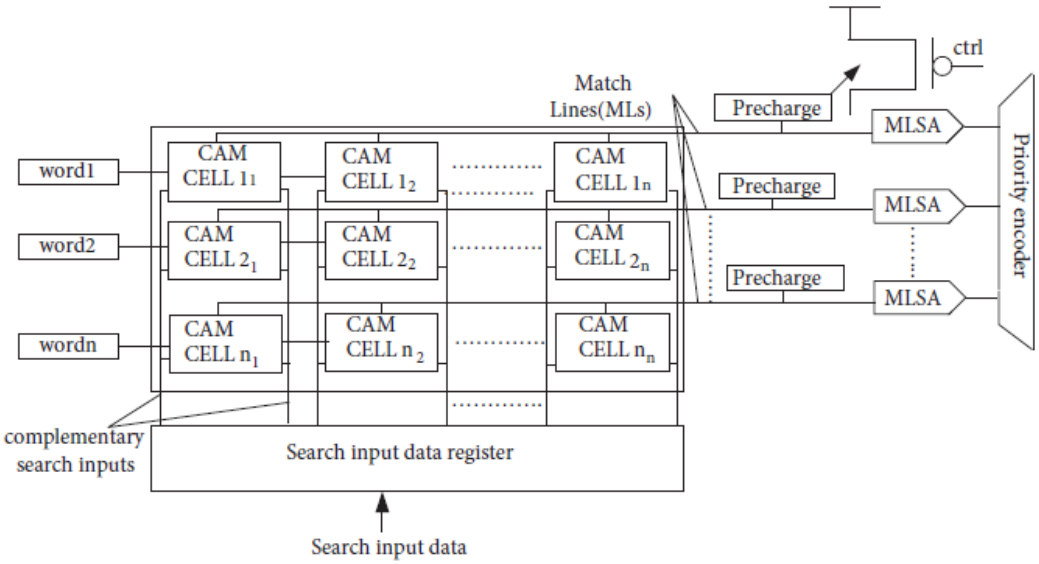

Fig.1 CAM design

2. Proposed Design:

The architecture of the proposed HSCPF CAM cell consists of a two 6T SRAM cells, with four NMOS transistors *M*7 , *M*8 , *M*17 , and *M*18 . We use a hybrid charge control circuitry, which controls two consecutive CAM cells. It consists of *M*9 and *M*10 transistors as shown in Fig.2. The gates of *M*9 and *M*10 transistors are connected to node *S*1 and the source of *M*10 transistor is connected to node *S*0 . In this charge control circuit, charge values at nodes *S*0 and *S*1 control the ML output for high or low. If the prestored data in two CAM cells is matched with the search input, the charge value at nodes *S*0 and *S*1 is high which in turn passes a high value to ML through transistors *M*9 and *M*10 , else it passes low value. These two CAM cells will be considered a CAM word for further operation. • All these CAM words are connected in parallel to constitute ML structure. If the search content matches with the prestored data in the first CAM word, the charge values at the nodes *S*0 and *S*1 are high. This process continues for the remaining CAM words in the ML structure until nodes *SN*□1 and *SN* . If all the prestored bits in a word are matched with the input search word, the ML attached to that word charges to high. In the case where prestored bits in a word are not matched with the input search word even by one bit, the ML attached to that word charges to low.

The architecture of the proposed HSCPF-CAM cell consists of a two 6T SRAM cell, with four NMOS transistors M_7, M_8 M_{17} and M_{18}. We use a hybrid charge control circuitry, which controls two consecutive CAM cells. It consists of M_9 and M_{10} transistors as shown in Fig.2 The gates of M_9 and M_{10} transistors are connected to node S_1 and the source of M_{10} transistor is connected to node S_0.In this charge control circuit, charge values at nodes S_0 and S_1 controls the *ML* output for high or low. If the pre-stored data in two CAM cells is matched with the search input, the charge value at nodes S_0 and S_1 is high which in turn passes a high value to *ML* through transistors M_9 and M_{10}, else it passes low value. These two CAM cells will be considered as a CAM word for further operation.All these CAM words are connected in parallel to constitute *ML* structure as shown in Fig2. If the search content matches with the pre-stored data in the first CAM word, the charge values at the nodes S_0 and S_1 are high. This process continues for the remaining CAM words in the *ML* structure till nodes S_{N-1} and S_N . If all the pre-stored bits in a word are matched with the input search word, the *ML* attached to that word charges to high. In case pre-stored bits in a word are not matched with the input search word even by one bit, the *ML* attached to that word charges to low. Table.1 shows the truth table of HSCPF-CAM cell for match/miss.

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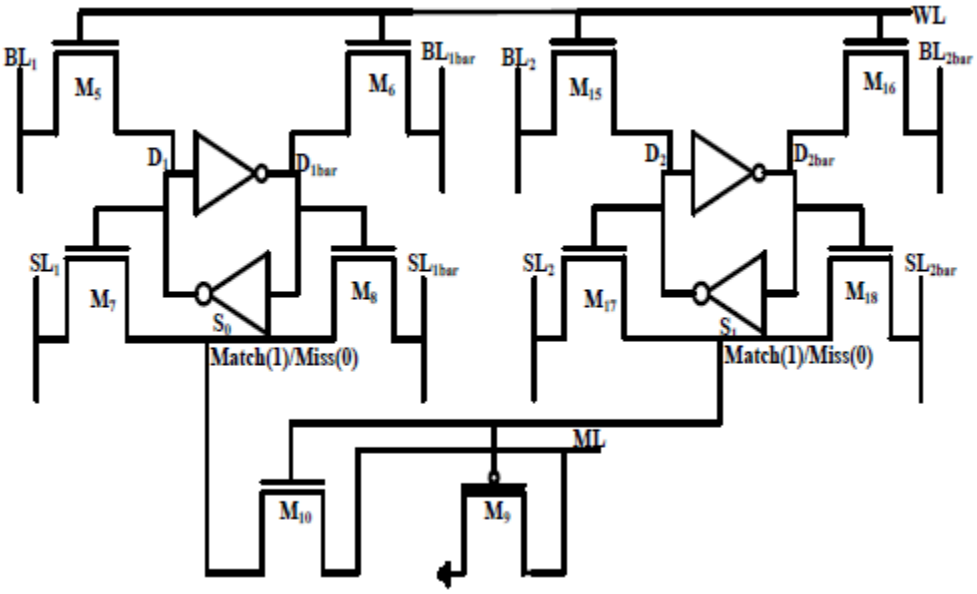

Fig.2. Proposed design

S0	S1	ML	output indicates
0	0	Miss	Low
0	1	Miss	Low
1	0	Miss	Low
1	1	match	High

Table.1 Truth table of HSCPF

3. Synthesis Results:

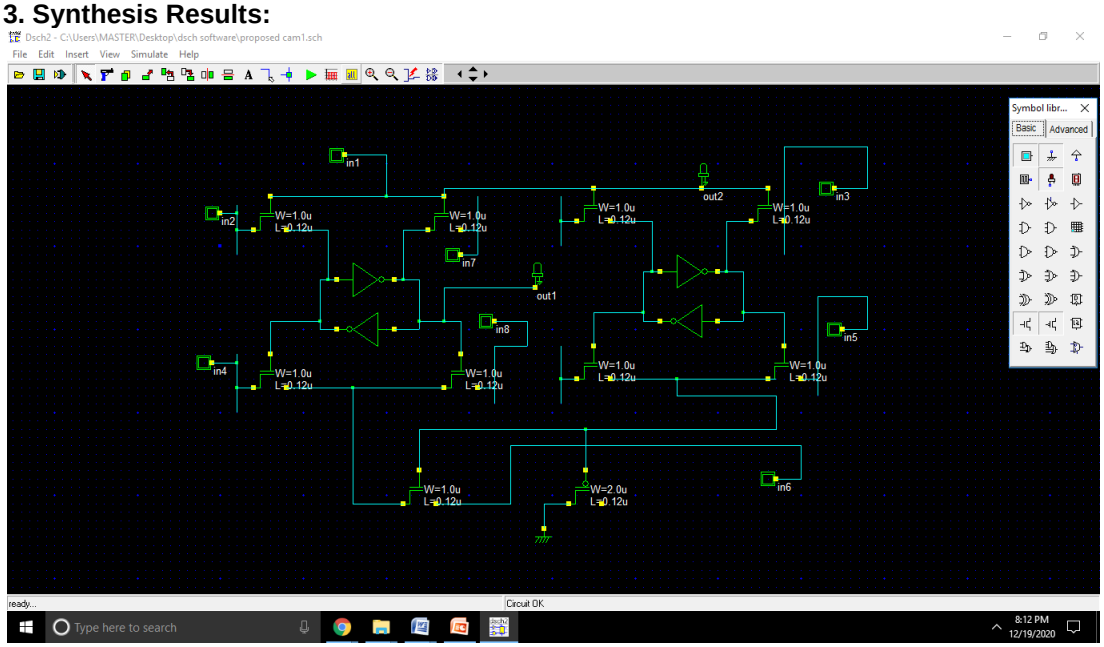

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Fig.3 Schematic of HFCPF

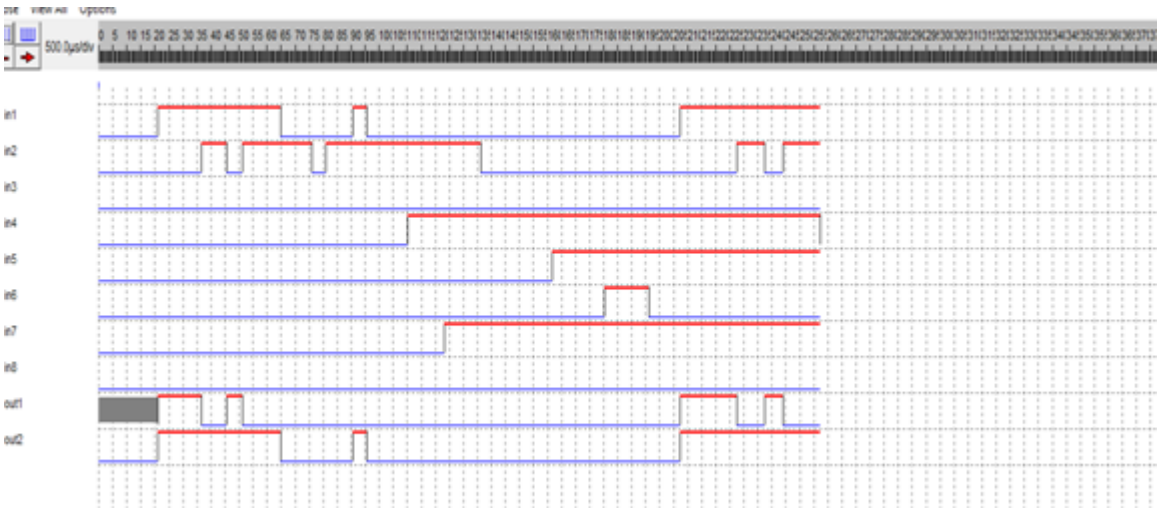

Fig.4 Simulation wave form

Fig.3 shows the proposed schematic circuit ad Fig.4 shows the wave forms of the read, write working operation of the circuit.

Conclusion:

In this dissertation, novel CAM cells and architectures with different storage cells, logics and devices are designed, simulated and the performance metrics are obtained. In these works, cadence tool is effectively used for the simulation of memory circuits for low power and high performance. Simulation results were validated with the conventional and existing CAM designs available in the literature, as result of which an assurance can be granted for the proposed CAM circuits designed. The following are the important conclusions that can be made for this paper.

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