ISSN: 2582 - 6379
Orange Publications
International Journal for Interdisciplinary Sciences and Engineering Applications
IJISEA - An International Peer- Reviewed Journal
2025, Volume 6 Issue 2
www.ijisea.org

Synthesis and Efficient Design of Reversible Serial Adder Based on EPOE Expressions

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ABSTRACT

The design of a low-cost self-control serial adder system is suggested in this project. The suggested circuit reduces the fixed inputs of sequential logic circuits by using EPOE expressions for the direct and compact design of sequential circuits. When it comes to energy-efficient calculations, reversibility is crucial. Common terms between the outputs are used as efficiently as possible to lower the quantum cost. The final circuit's quantum cost can be decreased by restricting the use of Toffoli gates larger than three inputs.

Keywords: Reversible, EPOEexpressions, Toffoligate, Fredkingate, Feynmangate, Double Peres gate,Garbage output.

Abbreviations: EPOE, Exor of Product of Exor's.

I.INTRODUCTION

Reversible computing is essential for low-power digital circuits, quantum computing, and nanotechnology because it preserves information and lowers energy dissipation. High-speed computing is impacted by irreversible logic, which loses information and produces heat of $kT\ln 2$ per erased bit, according to Landauer's principle. Bennett showed that by guaranteeing a one-to-one mapping between inputs and outputs, reversible logic prevents energy loss. Reversible gates (like Toffoli, Fredkin, and Feynman) allow computations to be reversed without wasting energy because they do not erase information like conventional gates (like NAND, OR, and EXOR) do.

Research aims to lower quantum cost, gate count, and garbage outputs in reversible circuits, which are crucial for arithmetic operations like multipliers, adders, and subtractors. Sequential logic powers the majority of modern computing, but switching from traditional latches and flip-flops to reversible alternatives presents problems like fixed inputs and high quantum cost. Reversible logic is still essential for quantum dot cellular automata, DNA computing, optical computing, and ultra-low-power VLSI.

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Heat loss has decreased due to fabrication advancements, but power consumption is rising as transistor density and clock speeds increase. Conventional computers lose information due to the irreversible nature of almost all logic gates, which causes heat dissipation. Reversible circuits guarantee that no energy is wasted by allowing computations to proceed both forward and backward.

For increased efficiency, researchers are still creating and refining reversible circuit designs. The suggested NS Gate (NSG) simplifies circuit design by showing how all Boolean operations can be carried out by a single reversible gate. Reversible logic provides a sustainable solution for next-generation computing, balancing performance and energy efficiency as the demand for fast, power-efficient systems increases. Reversible logic is anticipated to be essential to future computational developments due to its applications in quantum computing and nanotechnology.

II.LITERATURE REVIEW

In 2010 ,Lihui Ni et al. [3] proposed a general methodology for the synthesis of reversible full adders. an essential building block for quantum computing and low-power digital circuits. It used only two reversible gates like the Toffoli or Fredkin gates to build compact circuits with minimal garbage outputs and quantum cost. With optimized hardware complexity and improved performance, this technique greatly facilitated the design of less complex and efficient full adders in reversible logic.

In 2011, Nagapavani et al. [4] proposed a reversible 4-bit shift register design, a basic digital system component used for serial-to-parallel and parallel-to-serial data conversion. Their method improved the performance of shift register circuits by employing reversible logic gates, such as the reversible D flip-flop for SISO, SIPO, PISO, and PIPO configurations. This research identified the potential of reversible logic in designing energy-efficient and low-power registers.Similarly, Zhijin Guan et al. [5] also made a contribution by designing an Reversible Arithmetic Logic Unit (ALU) that minimized the bit requirement of the design at the cost of information bit reuse. Their technique was able to minimize power usage without losing any functionality of an ordinary ALU.

In 2012, T. Naga Babu et al. [6] presented reversible adder/subtractor circuits using DKG (Double-Controlled Toffoli Gate) and TSG (Toffoli and Fredkin) gates. Their work included notable improvements in hardware complexity, gate numbers, garbage outputs, and constant inputs. The improvement of full adder and subtractor circuits within reversible logic for greater overall efficiency in low-power and quantum computing was one major highlight of their paper.Another study in 2014 introduced a low-power multi-port SRAM. This structure helps to reduce disturbances during write operations and improves SNM [7]. This design reduces the number of transistors per cell, making it more compact and power-efficient.

In 2017, Dhoumendra Mandal et al. [22] investigated the issues related to the design of reversible serial adders. They discussed how minimizing the number of states in a state machine might affect output validity and pointed out the intricacies involved in creating efficient and effective control circuits for reversible logic. Their study pinpointed important issues that need to be resolved to improve the functionality and efficiency of reversible adders in quantum and classical computing systems.

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In 2017, A.V. Ananthalakshmi et al. [20] proposed a reversible floating-point square root design using the modified non-restoring algorithm. This method, which avoids restoring the remainder in each step, resulted in a design that minimized logical resources while maintaining efficiency in terms of power and area. The work was particularly valuable for reducing hardware requirements in reversible floating-pointoperations.

III.PROPOSED METHOD

The proposed work in this paper focuses on the design and synthesis of reversible circuits, particularly emphasizing the development of a reversible serial adder based on the Exclusive Product of Exponentials (EPOE) approach. Here are the key aspects of the proposed work.

1. Importance of Reversible Logic: Reversible logic circuits are crucial for quantum computing and low-power electronics as they prevent information loss and reduce energy consumption. This makes them suitable for energy-efficient systems, contrasting with traditional circuits that may lead to information loss and higher energy usage.

2. Optimization of Reversible Circuits: The paper improves upon the EPOE method for reversible circuit synthesis by incorporating common terms within output expressions. This approach minimizes constant inputs and quantum cost, leading to enhanced hardware efficiency. The focus is on reducing the complexity of the circuits while maintaining their functionality.

3. Use of Three-Input Toffoli Gates:To avoid exponential complexity in circuit design, the proposed work restricts the use of Toffoli gates to three inputs only. This limitation helps streamline the design process and contributes to lowering the overall quantum cost and hardware complexity of the circuits.

4. Application of the Serial Adder: A central application explored in the paper is the serial adder, which processes one bit at a time. While it may not be the fastest option available, it is cost-effective and conserves hardware resources, making it suitable for small quantum circuits. The proposed design aims to optimize the serial adder further by decreasing its quantum cost and hardware complexity.

5.Energy-EfficientCalculations: The proposed circuit design emphasizes energy-efficient calculations by leveraging the principles of reversibility. By efficiently utilizing common terms between outputs, the design aims to lower the quantum cost, which is critical for practical applications in low-power and quantum computing environments.

Gate Functionality in Reversible Logic

The Fredkin Gate is a controlled swap gate that swaps the values of the two inputs according to a control signal. In the above design, P1_BAR (¬A) is the control signal. When P1_BAR is 0, the gate swaps the content of R and C. When P1_BAR is 1, there is no swap, so the circuit can continue with addition or subtraction accordingly.

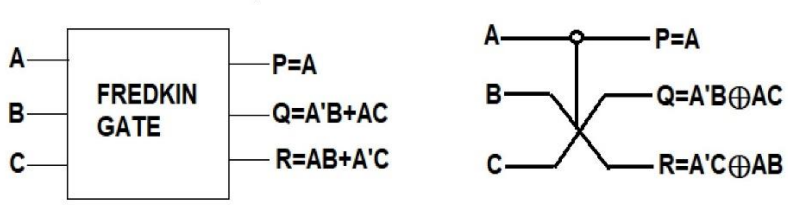

Figure 1: Block diagram Fredkin Gate

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The BORROW signal is important in establishing when subtraction must be performed. When a borrow is created when subtracting, the system performs the subtraction operation accordingly. Smooth transitions between addition and subtraction are facilitated by the Fredkin Gate through the utilization of carry and borrow signals and thus it forms an integral part of reversible arithmetic operations.

Double Peres Gate, NOT Gate, and Fredkin Gate are the building blocks of the reversible serial adder realized with EPOE expressions. Each is specially selected due to the capacity to facilitate addition and subtraction in a reversible fashion with no energy loss in computation. Conditional operations can be efficiently handled by the Fredkin Gate, whereas the Double Peres Gate and the NOT Gate are responsible for arithmetic and control operations. The combination of these gates forms a low-power, reversible, and efficient computing system well adapted to low-energy and quantum applications.

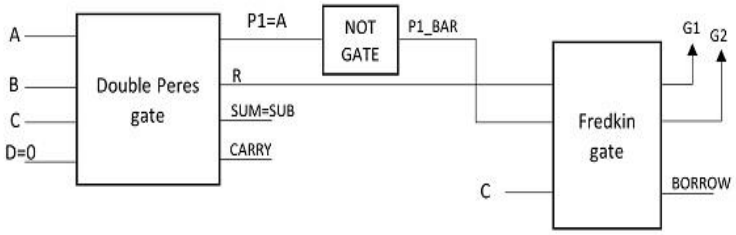

Figure 2: Internal circuit of FA/FS

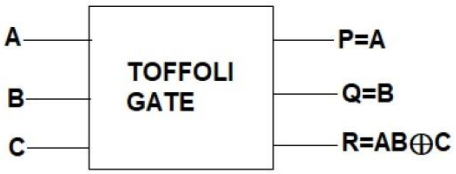

Figure 3 : Block diagram of Toffoli gate

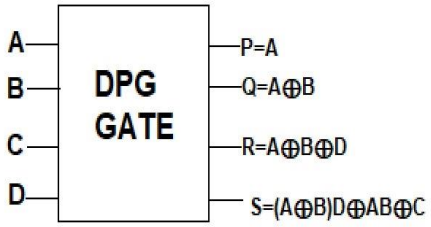

Figure 4: Block diagram of Double Peres Gate

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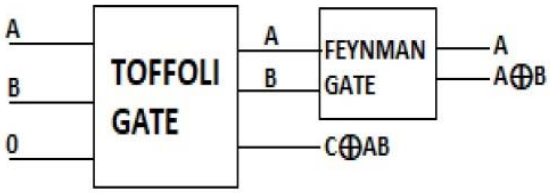

Figure 5: Half-adder using Toffoli (To) and Feynman (Fe) gate

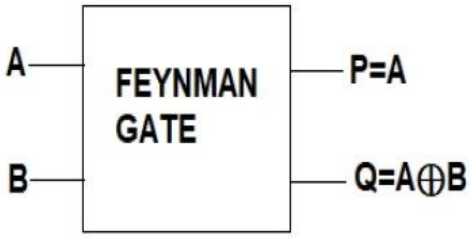

Figure 6: Block diagram of Feynman Gate

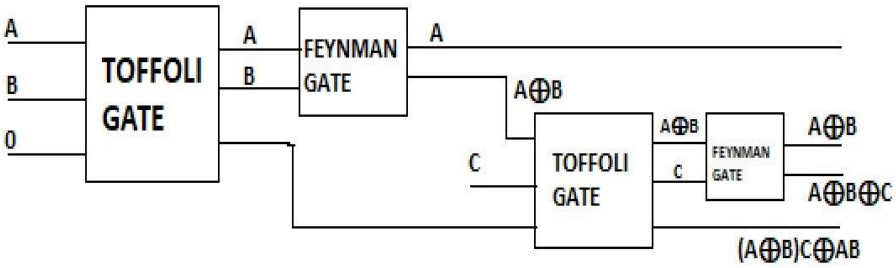

Figure 7: Full-adder using Toffoli (To) and Feynman (Fe) gate

Addition and Subtraction Operation in the Reversible Serial Adder

The reversible serial adder, which is built with EPOE expressions, carries out addition and subtraction by combining the Double Peres Gate, NOT Gate, and Fredkin Gate. The gates operate in conjunction to provide effective arithmetic operations with reversibility and energy loss reduction.

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The inputs to this circuit are A, B, and C, which enter the arithmetic process. The input A is used within the Double Peres Gate and also get negated via the NOT Gate to create control input for the Fredkin Gate. Inputs B and C join in the subtraction or addition operation, and the constant input D = 0 eases work in the Double Peres Gate.

The Double Peres Gate performs the initial sum (or difference) and carry bit computation. In addition, it calculates the sum of A, B, and C and produces a CARRY bit when the sum is greater than 1. In subtraction, the output is the difference of A, B, and C, with the CARRY bit being a borrow when required.

The NOT Gate inverts A and generates P1_BAR (¬A), a control signal used by the Fredkin Gate. The control signal decides whether an addition or a subtraction operation will be performed. If P1_BAR is 0, addition is performed; if P1_BAR is 1, subtraction is performed.

The Fredkin Gate, the three-input, three-output controlled swap gate, is responsible for choosing the arithmetic operation. In addition, when P1_BAR is 0, the Fredkin Gate passes the sum (R) and CARRY unaltered. Consequently, the outputs G1 and G2 are the sum, and the BORROW signal is inactive. In subtraction, when P1_BAR is 1, the Fredkin Gate exchanges R and CARRY, considering the CARRY bit as a borrow. Such a modification guarantees that the circuit properly calculates the difference, and the BORROW signal is triggered if so required.

The ultimate outcome of the operation depends on addition or subtraction. If there is no borrow, the outputs G1 and G2 hold the sum, and the BORROW signal is not active. If borrow is required, G1 and G2 hold the result of the subtraction, and the BORROW signal is asserted to indicate the process of subtraction.

By combining these reversible gates, the serial adder effectively manages both the arithmetic operations with minimal quantum cost and energy consumption, thereby being a suitable candidate for low-power and quantum computing applications.

Block Diagram of Self-Control Serial Adder/Subtractor

The self-controlled serial adder/subtractor has two primary components: the Adder/Subtractor Components and the Control Unit. The two components collaborate to execute both addition and subtraction processes in serial form.

The Adder/Subtractor Components comprise a full adder, full subtractor, D flip-flop, and 8-bit shift register. The full adder is tasked with adding two input bits and one carry-in bit from the preceding stage to produce a sum and a carry-out bit. The full subtractor also does subtraction using two input bits and a borrow from the preceding stage to produce the difference and borrow bits. Both full adder and full subtractor are used for efficient handling of arithmetic operations.

The D flip-flop is a crucial part of our sequential operations by maintaining the carry-out or borrow bit produced during every clock cycle. It helps ensure that the carry or borrow is ready for the subsequent operation to have continuous addition or subtraction without any errors.

The 8-bit shift register is another important component that keeps the intermediate results of addition and subtraction temporarily while enabling data to shift in and out sequentially. This allows the system to execute operands bit by bit, with smooth and systematic arithmetic computation.

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The Control Unit also oversees the overall operation of the adder/subtractor by producing three major control signals: Init, ShiftEn, and CountEn. The Init (Initialization) signal is used to reset all registers and parts and make them ready for computation. This avoids any discrepancies caused by carryover data from previous computations. The ShiftEn (Shift Enable) signal enables the operands to be shifted through the shift register so that each bit is processed in the right sequence in addition or subtraction. The CountEn (Count Enable) signal tracks the number of clock cycles so that the system knows when all the bits have been processed and when to stop the operation.

By combining these elements, the self-controlled serial adder/subtractor efficiently carries out sequential arithmetic functions. It is designed to have low power consumption, and hence it becomes ideal for low-power computing and reversible logic-dependent applications. The integration of a full adder, full subtractor, flip-flop memory, shift registers, and control unit enables efficient addition and subtraction operations in an orderly and error-free mode.

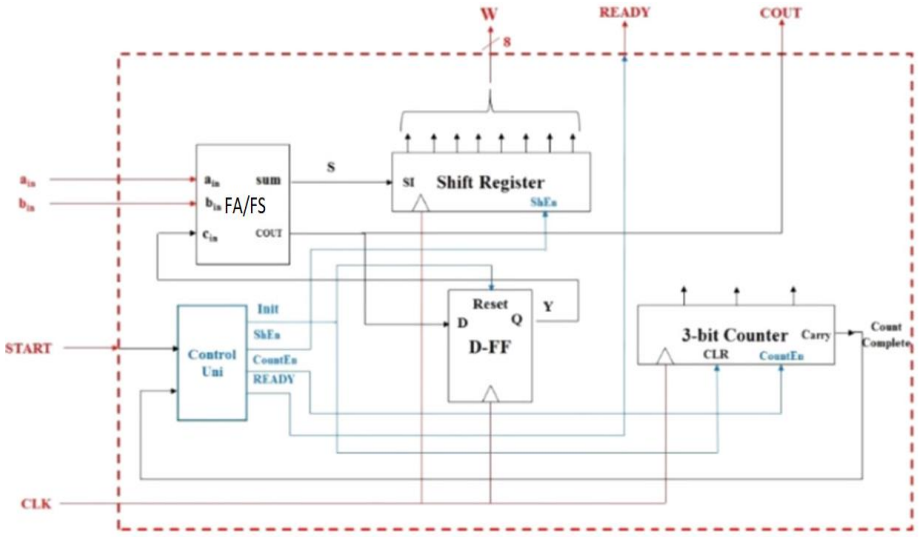

Figure 8: Block diagram of Serial adder/subtractor

IV.RESULTS AND DISCUSSION

The analysis of results compares the reversible serial adder based on EPOE Expressions in terms of Garbage outputs, Constant inputs, Quantum cost, Power consumption, Area utilization, and Timing performance. The analysis emphasizes the energy efficiency of reversible circuits, which makes them suitable for low-power, high-performance computing.

By contrast to traditional adders, we show power savings, area efficiency, and computation speed. The results highlight the promise of EPOE-based reversible adders for uses such as embedded systems, mobile terminals, and quantum computing, supporting their place in next-generation energy-efficient technology.

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Performance Metrics

1.Garbage Outputs: Reversible circuits produce additional bits that do not affect computation. Reducing these garbage outputs improves efficiency. Our analysis illustrates how EPOE expressions minimize this waste relative to traditional adders.

2.Constant Inputs: Constant inputs reduce circuit complexity and maximize performance. We analyze the effect of constant inputs in our design, noting their contribution to increased efficiency.

3.Quantum Cost: The quantum gate count decides the feasibility of a circuit for quantum computing. By comparing our design's quantum cost with conventional adders, we highlight its potential advantages in reversible and quantum logic.

3.Power Consumption: One of the main benefits of reversible logic is low power dissipation. Our analysis verifies that the EPOE-based reversible adder minimizes power consumption, making it suitable for energy-limited applications such as embedded systems and mobile phones.

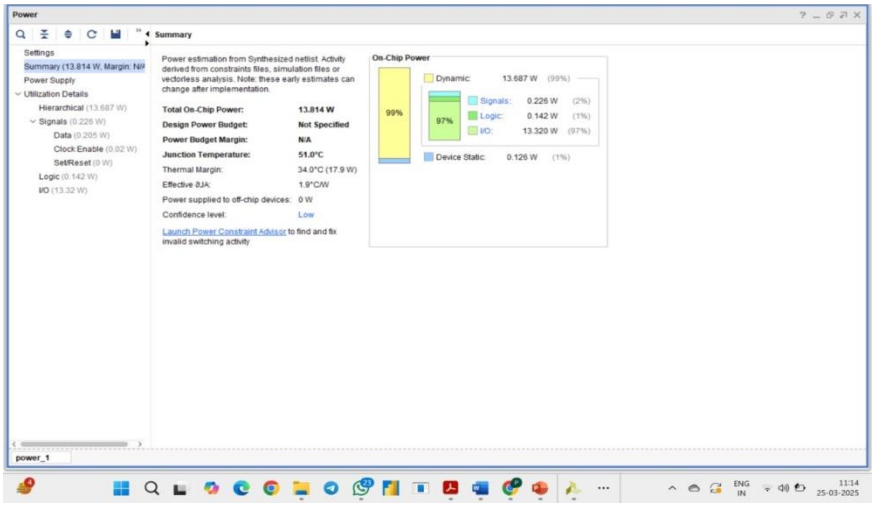

Figure 9: Power Analysis

4.Area Utilization: Hardware efficiency is area utilization-dependent. We compare the spatial footprint of our adder with traditional designs, showing an efficient balance between performance and resource utilization.

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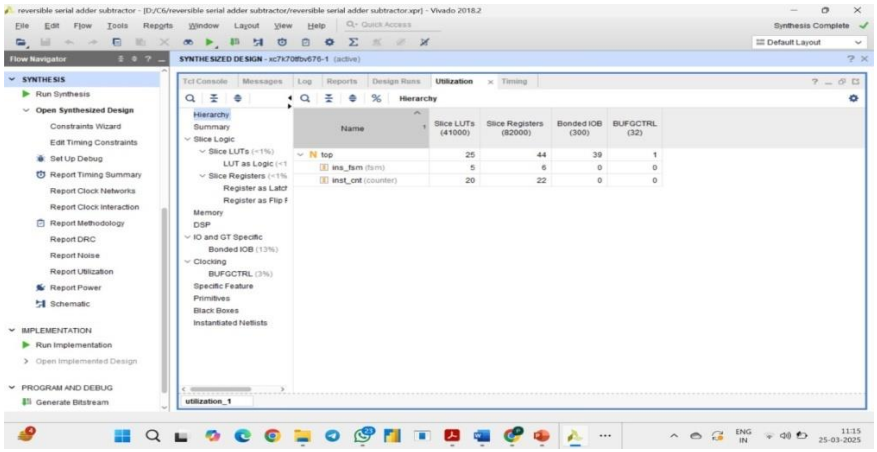

Figure 10: Area Utilization

5.Timing Performance: Our timing analysis assesses delay on the critical path and computational speed. The outcome indicates that our design has high-speed processing with minimal power consumption, which makes it highly applicable in high-performance applications.

Through these fundamental parameters, we conclude that the EPOE-based reversible serial adder is a power-efficient, scalable, and high-performance computation solution for contemporary computing demands.

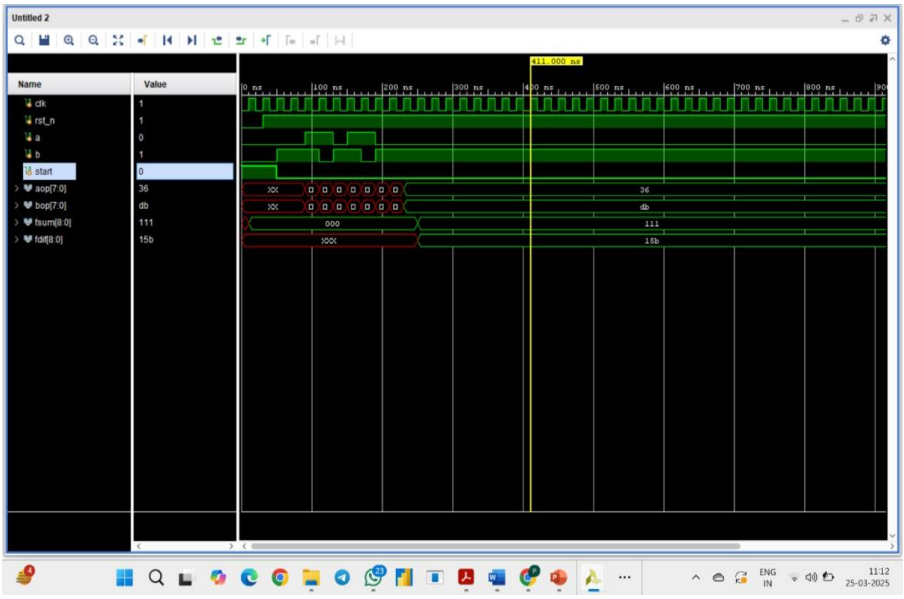

Figure 11: Simulation Result of Full Adder/Full Subtractor using Vivado software

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The above waveform illustrates the functional verification of a reversible logic circuit under test. The key signals observed are clk, rst_n, a, b, start, and the resulting outputs: apop[7:0], bop[7:0], fsum[8:0], and fdiff[8:0].

Initially, the system is held in reset (rst_n = 0), ensuring all outputs remain undefined (XXX). Upon releasing the reset (rst_n = 1), the inputs a = 0 and b = 1 are fed into the system. The start signal is asserted and then deasserted, signaling the system to begin computation.

Once the logic is triggered, the following outputs are observed at around 411 ns:

apop[7:0] = 36,bop[7:0] = db,fsum[8:0] = 111,fdiff[8:0] = 15b

These values indicate the processed outputs of the operands a and b through the reversible logic unit. Specifically:

The apop and bop signals represent processed (possibly encoded or transformed) versions of inputs a and b.fsum and fdiff represent the reversible full-adder/subtractor outcomes in 9-bit format. The stable output signals and absence of undefined states post-reset confirm that the circuit functions correctly and transitions to valid output states after computation. The simulation demonstrates correct behavior and timing alignment as per the design specifications.

Description about Simulation

1. clk (clock): The first signal shown is a clock (clk), which is typically used to synchronize other signals in a digital circuit. It appears as a square wave, changing between 0 and 1.
2. rst_n (reset): This signal seems to be a reset, with a value of 1 initially, indicating that the system is not in a reset state, and it is later de-asserted.
3. a, b: These are inputs to the system. Their values are shown as respectively.
4. start: A control signal, likely used to trigger some operation. Its value is 0 in the simulation.
5. aop[7:0]: This seems to be an 8-bit signal.
6. bop[7:0]: Another 8-bit signal.
7. fsum[8:0]: This signal seems to represent the sum or result of an operation.
8. fdiff[8:0]: This likely represents the difference between two values.

Table 1 : Results Comparision with existing system

Parameters	Proposed System	Existing System [1]	Existing System [24]
Constant Inputs	1	1	4
Garbage Outputs	2	4	2
Quantum Cost	7	17	29
Power Consumption	13.514W	13.687W	36.43W
Timing Summary	34.19ns	37.933ns	58.058ns
Gate Count	109	113	125

The proposed system shows significant improvements over Existing System and Existing System across key performance metrics. It uses only one constant input and generates just two garbage outputs, ensuring minimal resource usage. With a quantum cost of 7, it is far more efficient than System and System making

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it well-suited for quantum logic applications. The power consumption is the lowest at 13.514W, and it also achieves the fastest performance with a delay of 34.19ns. Additionally, the proposed system has the least gate count (109), indicating reduced complexity and better scalability. Overall, it provides a highly optimized and energy-efficient solution compared to the existing designs.

V.CONCLUSIONS

This paper, Design of Reversible Serial Adder Based on EPOE Expressions for Computational Applications, discusses an energy-efficient serial adder that uses reversible logic and EPOE expressions. The design saves a lot of power consumption, heat dissipation, and hardware complexity and is suitable for low-power and high-performance systems.

By using EPOE phrases, the adder maximizes resource utilization and offers an efficient solution for applications that need precision and scalability, including digital signal processing and embedded systems. The outcomes confirm the viability of the approach and render it a good candidate for energy-conscious and quantum computing applications..

In contrast to the Low Power Reversible Parallel Binary Adder/Subtractor, this design provides lower complexity, higher scalability, and better energy efficiency. Its power minimization capabilities at the cost of latency and hardware overhead make it specifically appropriate for embedded systems and Internet of Things devices, where efficiency, power, and area requirements are main concerns.

Advantages

1.Energy Efficiency and Power Reduction.
2. Improved Computational Efficiency.
3. Reduced Heat Dissipation.
4. Quantum Computing Support.
5. Optimized Resource Utilization.
6. Compatibility with DSP Applications

Applications

1. Low-power computational devices.
2. Quantum computing circuits.
3. Digital signal processing.
4. Embedded system designs.
5. Energy-efficient hardware design.
6. High-performance computing systems.

Future Scope

The EPOE-expression-based reversible serial adder opens the door for several exciting avenues of research. One important direction is integration into quantum computing, where optimizing the design to suit quantum gates will boost circuit efficiency. Optimizing speed is another important thrust, which can minimize timing delays and enhance the critical path, making the adder suitable for high-speed applications like cryptography and signal processing.

Increased scalability will allow the adder to support complex calculations in high-end systems. Its potential also lies in machine learning and AI, where energy-efficient hardware may accelerate data-intensive computations. Improving fault tolerance and adding error correction mechanisms will make it more reliable, especially for safety-critical systems.

In addition, hardware-software co-design can maximize overall system performance, and new logic gate designs and other EPOE expressions could further minimize garbage outputs and power consumption. As these developments continue, the reversible serial adder will continue to be an important building block in low-power, high-performance computational systems in many fields.

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